## IN THE CLAIMS

Please amend the claims as follows:

1. (Previously Presented) A method, comprising:
recording an address of a write operation to a memory having information cached by a non-volatile cache prior to executing an operating system cache driver associated with the non-volatile cache.

2. (Original) The method of claim 1, wherein recording the address of the write operation further comprises:
recording the address in a log.

3. (Original) The method of claim 2, wherein the log is stored in a memory comprising at least one of a static random access memory (SRAM), a dynamic random access memory (DRAM), a flash memory, and a polymer ferroelectric RAM (PFRAM).

4. (Original) The method of claim 1, further comprising:
detecting the write operation.

5. (Original) The method of claim 4, wherein detecting the write operation further comprises:
trapping an interrupt request.

6. (Original) The method of claim 1, further comprising:
modifying data corresponding to the address of the write operation.

7. (Original) The method of claim 6, wherein modifying the data corresponding to the address of the write operation further comprises:
updating the data corresponding to the address of the write operation.

8. (Original) The method of claim 6, wherein modifying the data corresponding to the address of the write operation further comprises:

invalidating the data corresponding to the address of the write operation.

9. (Previously Presented) An article comprising a machine-accessible medium having associated data, wherein the data, when accessed, results in a machine performing:

recording an address of a write operation to a memory having information cached by a non-volatile cache prior to executing an operating system cache driver associated with the non-volatile cache.

10. (Previously Presented) The article of claim 9, wherein the data, when accessed, results in the machine performing:

recording the address of the write operation in a log.

11. (Original) The article of claim 10, wherein the log is included in a non-volatile memory.

12. (Original) The article of claim 10, wherein the data, when accessed, results in the machine performing:

setting a flag to indicate an overrun of the log.

13. (Currently Amended) The article of claim 12, wherein the data, when accessed, results in the machine performing:

invalidating the information ~~non-volatile cache~~ if the flag is set.

14. (Previously Presented) An apparatus, comprising:

a non-volatile cache; and

a memory to store an address associated with a write operation to a memory having information cached by the non-volatile cache prior to executing an operating system cache driver associated with the non-volatile cache.

15. (Original) The apparatus of claim 14, wherein the address is a logical block address.

16. (Previously Presented) The apparatus of claim 14, wherein the memory to store an address comprises a non-volatile memory.

17. (Original) The apparatus of claim 14, further comprising:
a module to receive an interrupt request associated with the write operation.

18. (Original) The apparatus of claim 17, wherein the interrupt request is a basic input-output system Int13h request.

19. (Previously Presented) A system, comprising:
a non-volatile cache; and
a memory to store an address associated with a write operation to a memory having information cached by the non-volatile cache prior to executing an operating system cache driver associated with the non-volatile cache;
a processor coupled to the memory to store an address; and
a display coupled to the processor.

20. (Original) The system of claim 19, further comprising:
a module to receive an interrupt request associated with the write operation.

21. (Original) The system of claim 20, wherein the module is included in a device option memory.

22. (Original) The system of claim 20, wherein the module is included in a basic input-output system.

23. (Previously Presented) The system of claim 19, wherein the memory to store an address comprises a non-volatile memory to store a log including a plurality of memory addresses including the address of the write operation.